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107. A method for making an insert for electrically interfacing an electronic device to a support substrate, the electronic device containing a plurality of contact bumps and a protrusion, the support substrate containing a plurality of conductive members, the insert having first and second sides, the method comprising:

(a) providing an insert substrate;

(b) forming in the first side of the insert substrate a plurality of pockets configured to receive and contact the contact bumps;

(c) forming in the first side of the insert substrate a recess configured to receive the protrusion when the contact bumps are received in the plurality of pockets;

(d) forming a dielectric material over the pockets; and

(e) forming a conductive material over the dielectric material and within at least some of the plurality of pockets.

108. The method of claim 107, further comprising forming a plurality of vias extending through the insert substrate to the second side which are in electrical communication with at least some of the plurality of pockets.

109. The method of claim 108, further comprising forming a plurality of conductive projections at the second side in electrical communication with at least some of the plurality of vias, the conductive projections receivable by at least some of the plurality of conductive members.

110. The method of claim 109, wherein the conductive projections are formed by:

(a) forming a stencil on the second side, the stencil containing holes at the vicinity of the vias;

(b) filing the holes with a conductive substance; and

(c) removing the stencil.

111. The method of claim 110, wherein the holes are filed with a melted conductive substance.

112. The method of claim 111, further comprising drawing a blade across a surface of the stencil to remove excess melted conductive substance from the stencil surface.

113. The method of claim 110, further comprising heating the conductive substance to form a bump.

114. The method of claim 107, wherein the insert substrate comprises a monocrystal.

115. The method of claim 114, wherein the monocrystal comprises silicon.

116. The method of claim 107, wherein the recess is formed to receive the protrusion with clearance when the contact bumps are received in the plurality of pockets.

117. The method of claim 107, wherein the pockets and the recess are formed to substantially the same depth.

118. The method of claim 117, wherein the pockets and the recess are formed simultaneously.

119. The method of claim 107, wherein the conductive material comprises at least one of the group consisting of refractory metal, refractory metal nitride, and refractory metal salicide.

120. The method of claim 109, further comprising forming a dielectric material between (i) the via and the insert substrate, and (ii) the conductive projections and the insert substrate.

121. The method of claim 120, wherein the dielectric material is silicon dioxide.

122. The method of claim 107, wherein the pockets are formed with walls sloped at an angle of about 40-70 degrees relative a plane defined by said substrate.

123. The method of claim 109, wherein the conductive projections comprise solder and are capable of being melted and adhered to the conductive members.

124. The method of claim 109, wherein the conductive projections are bumps.

125. The method of claim 107, wherein the pockets and the recess are formed using a wet etchant.

126. The method of claim 120, wherein the wet etchant comprises potassium hydroxide.

127. A method for making an insert for electrically interfacing an electronic device to a support substrate, the electronic device containing a plurality of contact bumps and a protrusion, the support substrate containing a plurality of conductive members, the insert having first and second sides, the method comprising:

(a) providing an insert substrate;

(b) forming in the first side of the insert substrate a plurality of pockets configured to receive and contact the contact bumps;

(c) forming a plurality of vias through the insert substrate to the second side which are in electrical communication with at least some of the plurality of pockets;

(d) forming a stencil on the second side of the insert substrate, the stencil containing holes at the vicinity of the vias;

(e) filing the holes with a conductive substance; and

(f) removing the stencil to form conductive projections in electrical communication with the vias and receivable by the conductive members.

128. The method of claim 127, wherein forming the vias involves the use of a laser.

129. The method of claim 127, wherein the holes are filed with a melted conductive substance.

130. The method of claim 129, further comprising drawing a blade across a surface of the stencil to remove excess melted conductive substance from the stencil surface.

131. The method of claim 127, further comprising heating the conductive projections to form a bump.

132. The method of claim 127, wherein the insert substrate comprises a monocrystal.

133. The method of claim 132, wherein the monocrystal comprises silicon.

134. The method of claim 127, further comprising forming in the first side of the insert substrate a recess configured to receive the protrusion when the contact bumps are received in the plurality of pockets.

135. The method of claim 134, wherein the recess is formed to receive the protrusion with clearance when the contact bumps are received in the plurality of pockets.

136. The method of claim 134, wherein the pockets and the recess are formed to substantially the same depth.

137. The method of claim 134, wherein the pockets and the recess are formed simultaneously.

138. The method of claim 127, further comprising forming a dielectric material in the plurality of pockets.

139. The method of claim 138, further comprising forming a dielectric material between (i) the via and the insert substrate, and (ii) the conductive projections and the insert substrate.

140. The method of claim 138, further comprising forming a conductive material over the dielectric material and within at least some of the plurality of pockets.

141. The method of claim 140, wherein the conductive material comprises at least one of the group consisting of refractory metal, refractory metal nitride, and refractory metal salicide.

142. The method of claim 138, wherein the dielectric material is silicon dioxide.

143. The method of claim 127, wherein the pockets are formed with walls sloped at an angle of about 40-70 degrees relative a plane defined by said substrate.

144. The method of claim 127, wherein the conductive projections comprise solder and are capable of being melted and adhered to the conductive members.

145. The method of claim 109, wherein the conductive projections are bumps.

146. The method of claim 134, wherein the pockets and the recess are formed using a wet etchant.

147. The method of claim 146, wherein the wet etchant comprises potassium hydroxide.